a mask ROM, which is formed in the semiconductor substrate, when the CPU executes a jump instruction in the first program;

executing the second program by the CPU to perform writing to the electrically programmable ROM by the CPU executing the second program; and

changing the process of the CPU executing the second program to the process for executing the first program when the CPU executes a return instruction in the second program,

wherein the memory and the EEPROM are allocated in mutually different addresses in one address space.

REMARKS

Claims 21, 24, 28 and 30 have been amended. No claims have been canceled or added. Accordingly, claims 21-30 are currently pending in the application.

Applicants appreciate the Examiner's acknowledgement of the claim for priority and safe receipt of the certified priority document filed in a parent application.

The claims have been amended to overcome the Examiner's objection.

Claims 21, 22, 24, 25 and 27-30 stand rejected under 35 U.S.C. §102 as being anticipated by Ugon. Claims 23 and 26 stand rejected under 35 U.S.C. §103 as being unpatentable over Ugon. These rejections are traversed as follows.

The present invention is directed to an electrically programmable ROM in which memory is allocated in mutually different addresses in a single address space. The first program that is stored in the electrically programmable ROM includes an instruction which changes the process of the CPU to one that controls the writing of the electrically programmable ROM according to a second program stored in the memory. The second program includes an instruction which returns the CPU to a process based on the first program after completion of the process that controls the writing of the ROM.

On the other hand, Ugon discloses a single chip microprocessor with an on-chip modifiable memory. As shown in Figures 2 and 3 and disclosed in the specification from column 5, line 55 to column 6, line 68, the memory 101 is divided into two memory blocks M1 and M2. Memory block M1 is addressed by register A1 102 and memory block M2 is addressed by register A2 103. Applicants wish to point out that although the Examiner refers to EPROM 101, it should be noted that memory 101 is formed from two blocks M1 and M2. Block M1 can be produced in the form of a read only memory (ROM) as recited in column 6, lines 6-7. On the other hand, the second memory block M2 must necessarily be in the form of a PROM or EPROM, as stated in column 6, lines 9-11. Memory block M1 contains all of the non-evolving programs or portions of the

program. Memory block M2 contains the evolving programs or portions of the programs, as recited in column 6, lines 3-5. Memory block M1 is coupled to data bus BUS D via address register A2 103 and via data register D 106, as recited in column 6, lines 23-26.

Thus, address register A1 102 is a program counter and data register IR is an instruction register as presumed by one of ordinary skill in the art. Therefore, memory block M1 is a program memory containing the main program of the microprocessor. This means that the main program including the CALL PROG referred to at column 7, line 65 is contained in memory block M1. It follows that the write program PROG and the main program are contained in memory block M1.

The Examiner maintains that the evolving or instructions, including a processing program, are stored in section M2 which has a first region to store a user program. Applicants respectfully disagree. There is no disclosure by Ugon that the instructions are a processing program. The Examiner may have assumed that the instructions in section M2 correspond to "the main program" recited in column 7, line 55 and believed that it corresponded to "the user program" or "the first program" recited in the pending claims. However, there is no such disclosure made by Ugon.

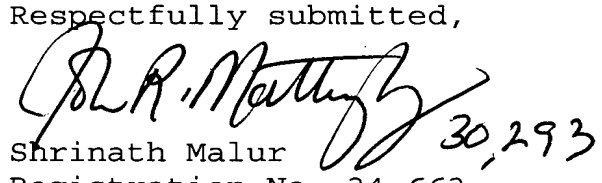
Additionally, one having ordinary skill would assume that memory block M1 and memory block M2 are allocated at different

address spaces, since they are accessed by respective address signals stored in address registers A1 102 and A2 103. As shown in Figures 1 and 2 of Ugon, memory block M1 is connected to address bus A1 and data bus B1 while memory block M2 is connected to address bus A2 and to data bus D2.

On the other hand, according to the present invention, the ROM and the memory are allocated at mutually different addresses in one address space from which the central processing unit can be accessed. Such a common bus structure has been inserted into the claims by this amendment. The bus structure of Ugon is different from the common bus structure of the present invention and therefore, the pending claims patentably define the present invention over Ugon.

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is now in condition for allowance. Reconsideration and reexamination are respectfully requested.

Respectfully submitted,



Shrinath Malur 30,293
Registration No. 34,663
Attorney for Applicants

MATTINGLY, STANGER & MALUR
104 East Hume Avenue
Alexandria, Virginia 22301
(703) 684-1120
Date: November 20, 2000